REMARKS

The independent claims have been amended better to point out that which applicant regards as his invention. More particularly, the claims have been revised to state that the connection members extend in a direction perpendicular to the semiconductor chip, have a longitudinal shape, and have an area of contact with the wiring layer that is less than an area of contact with an electrode. Such configuration can clearly be seen from a review of Figs. 1 to 8 in this case.

Two new claims (16 and 17) have been added specifying that the wire bump is a gold wire bump; support for this claimed feature can be found in the specification at least at page 5, line 31. The claims before the Examiner thus are claims 1 to 17.

Enclosed herewith is a Request for Approval of Drawing Change. One request relates to Fig. 2 to supply a parenthetical and a numeral 30 similar to the arrangements depicted in Figs. 3 and 4. Fig. 9 is requested to be changed to designate prior art.

The rejection of what is assumed to be claims 1 to 4 and 6 under 35 USC 102 as anticipated by Chakravorty '569, if applied to claims 1 to 4, 6, and 16, is respectfully traversed. There is no showing in the reference of a member connecting the semiconductor

chip electrodes and the wiring layer wherein those connection members extend in a direction perpendicular to the semiconductor chip, have a longitudinal shape, and have an area of contact with the wiring layer that is less than are area of contact with an electrode. Moreover, the bumps 311 shown in Chakravorty '569 correspond to bumps 70 in the instant drawings and are not the connection members 30 or 31 shown in the instant application. The instant invention represents a distinct improvement over the prior art, particularly over semiconductor devices such as shown in Fig. 9 with rigid and thick posts 150. There are significant and patentable differences between this prior art configuration that shown in Chakravorty '569 and what is claimed herein. The elements in the Chakravorty '569 device that may said to be closest in function to the connecting members of the present claims are the V-shaped portions with extended bottoms of metal traces 307. Those elements in no way teach or suggest the connection members of the present claims. Moreover, the reference elements cannot be said to achieve the objectives of the present invention, wherein the connection members of the claims aid to resist cracks and warps in the semiconductor chips to occur even during temperature changes. Applicant points out at page 5, lines 33 to 36 of the specification

that the connection members of the present claims can be deformed and thus mitigate thermal stresses to which the semiconductor device is subjected. Chakravorty '569 provides no such advantage. The rejection should be withdrawn.

The rejection of claim 5 under 35 USC 103 as unpatentable over Chakravorty '668 in view of Inaba et al. '734 is respectfully traversed.

Chakravorty '668 is a divisional patent of Chakravorty of '569 and contains essentially the same text. The deficiencies of Chakravorty '668 are identical to those discussed above with respect to Chakravorty '569. Inaba et al. '734 has been cited in this rejection merely to show a solder resist layer. That teaching without more does not overcome the deficiencies of the primary reference discussed and the rejection should be withdrawn. None of these cited references teaches or suggests a connection member of the instant claims.

The rejection of claims 7 to 15 under 35 USC 103 as unpatentable over Inaba et al. '734 in view of Chakravorty '668, if applied to claims 7 to 15 and 17, is respectfully traversed.

It is asserted in the Office Action that the primary reference shows all the claimed subject matter but for forming individual

semiconductor chips. Applicant respectfully disagrees. The techniques described in Inaba et al. '734 do not include the formation of a connection member having the shape and manner of attachment recited in the independent claim and the rejection should be withdrawn. The secondary reference having been cited merely to show a method of forming individual chips from a wafer; the manufacturing method of Inaba et al. '734 is not that of claims 7 to 15 and 17.

Applicant also seeks clarification regarding the receipt of a certified copy of the Japanese priority document. There was no check in any of the boxes numbered 1, 2, and 3 in the Office Action Summary. Clarification is requested.

In view of the foregoing revisions and remarks, it is respectfully submitted that claims 1 to 17 are in immediate condition for allowance and a USPTO paper to those ends is earnestly solicited.

The Examiner is requested to telephone the undersigned if additional changes are required in the case prior to allowance.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

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Date

Charles A. Wendel
Registration No. 24,453

CAW/ch

Attorney Docket No.: DAIN:644

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220

Serial No. 09/917,854

MARK UP CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor chip having electrodes;

an insulation layer formed on a surface of the semiconductor chip where the electrodes of the semiconductor chip are formed; and

a wiring layer formed on the insulation layer,

the electrodes of the semiconductor chip and the wiring layer being connected to each other via connection members disposed in the insulation layer wherein said connection members extend in a direction perpendicular to the semiconductor chip, have a longitudinal shape, and have an area of contact with the wiring layer that is less than an area of contact with an electrode.

7. (Amended) A method for fabricating a semiconductor device comprising the steps of:

preparing a wafer including a plurality of semiconductor chips with electrodes formed [on] thereon;

forming connection members on the electrodes of the respective semiconductor chips, the connection members extending in a direction

perpendicular to the semiconductor chps and having a longitudinal shape and an area of contact with a herein later identified wiring layer that is less than an area of contact with an electrode;

forming an insulation layer in a thickness to cover the connection members on the surfaces of the respective semiconductor chips where the electrodes of the semiconductor chips are formed;

polishing the insulation layer to expose the connection members;

forming an electroless plated layer on the insulation layer; and

forming, with the electroless plated layer as a feeder layer of electric current, an electrolytic plated layer on the electroless plated layer selectively only in regions for a wiring layer;

etching off the electroless plated layer except regions of the electroless plated layer corresponding to the electrolytic plated layer to form the wiring layer including the electroless plated layer and the electrolytic plated layer; and

severing the wafer into the respective semiconductor chips to fabricate the semiconductor device.